**Group 24**

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**Lab 1: g24\_num1s**

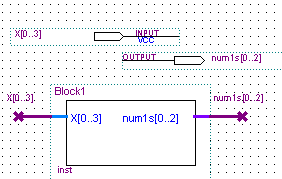
Circuit: g24\_num1s

Inputs: X- a 4 bit vector

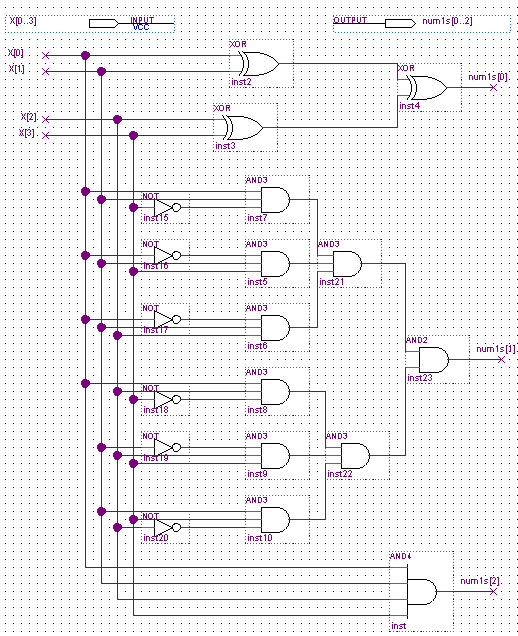
Outputs: num1s - a 3 bit vector

Function: This circuit takes a X from values from 0000 to 1111 and returns a count of the number of 1s in the vector num1s. Num1s is a 3 bit vector can have values from 0 to 100.

Circuit Diagram:



Gate level schematic diagram:



At gate level, the 4 bits of X are XORed to get the least significant bit of num1s so that the LSB is only one if the number of ones is odd. For the MSB, the 4 bits are ANDed together since it can only have a value of one if X has 4 ones.The middle bit is only set if there are 2 or 3 ones and the minimal SOP form of the Karnaugh map for nums[1] is used.

This circuit was tested by simulating through all possible values of X and checking the values of num1s. It was correct since the values of num1s were as expected for each value of X.

We simulated through all possible X values from 0000 to 1111. Simply by checking the X’s number of ones and seeing if that total matched the output value for each test case we can conclude that the circuit functions properly with correct logic. For example we can see in the first waveform simulation picture below that at 30ns that there are two 1’s in 0011. Thus, our expected output would be the base 10 value 2 and in fact our output is 0010 which is equivalent to base 10 value 2.

Waveform simulations:

